

## WHAT IS CLAIMED IS:

1. A substrate processing system including first to n-th processing units ( $n = 1, 2, \dots, N$ ) each having at least one identical unit for performing first to n-th wafer-processing for given periods  $t_1$  to  $t_n$ , respectively, the processing being performed in order from the first unit to the n-th unit, a plurality of substrates being simultaneously processed by different types of the processing units for one cycle, the system comprising:

a loading/unloading section for taking in and out the substrates;

a first transfer section for receiving/transferring the substrates from/to the loading/unloading section and transferring the substrates one by one to each processing unit; and

a controller for controlling the first transfer section and the processing units so that each processing unit processes the substrates one by one in accordance with one-cycle time as a standard time, the one-cycle time being the maximum period among periods  $t_1/m$  to  $t_n/m$  obtained by dividing the periods  $t_1$  to  $t_n$  by the number "m" of the identical units of the first to n-th processing units.

2. The substrate processing system according to claim 1, wherein

the controller controls the first transfer section and the processing units so that the processing time required for each processing unit corresponds to the one-cycle time.

3. The substrate processing system according to claim 2, wherein

the processing time required for each processing unit includes a pre-transfer time, a net processing time, a post-transfer time and a plurality of waiting times.

4. The substrate processing system according to claim 3,

wherein

the waiting times are allocated before or after one of the pre-transfer time, the net processing time and the post-transfer time in the processing time required for each processing unit.

5. The substrate processing system according to claim 1, wherein

the controller controls the first transfer section and the processing units so that the processing time required for each processing unit corresponds to division of the one-cycle time by an integer.

6. The substrate processing system according to claim 5, wherein

the processing time required for each processing unit includes a pre-transfer time, a net processing time and a post-transfer time.

7. The substrate processing system according to claim 6, wherein

the processing time required for a desired processing unit further includes a waiting time.

8. The substrate processing system according to claim 1, wherein

the controller controls the first transfer section and the processing units so that the total of the processing times for the successive "n" number of processing units equals to one-cycle time x n.

9. The substrate processing system according to claim 8, wherein

the processing time required for each processing unit includes a pre-transfer time, a net processing time and a post-transfer time.

10. The substrate processing system according to claim 9, wherein  
the processing time required for a desired processing unit further includes a waiting time.

11. The substrate processing system according to claim 1, wherein  
the processing units include at least one thermal processing unit.

12. The substrate processing system according to claim 11, wherein  
the thermal processing unit has a heating mechanism and a lift-up mechanism for holding each substrate so that the substrate is distant from the heating mechanism, the thermal processing unit waiting for thermal processing while the lift-up mechanism is holding the substrate as distant from the heating mechanism.

13. The substrate processing system according to claim 1, wherein  
the processing units include one developing unit for developing a resist applied onto each substrate.

14. The substrate processing system according to claim 1, wherein  
the processing units include at least one exposing apparatus for exposing a resist applied onto each substrate.

15. The substrate processing system according to claim 1 further comprises  
a second transfer section accessible to each of the processing units for transferring each substrate from one of the processing units to another.

16. A substrate processing system including first to n-th processing units ( $n = 1, 2, \dots, N$ ) each having at least

one identical unit for performing first to n-th wafer-processing for given periods  $t_1$  to  $t_n$ , respectively, the processing being performed in order from the first unit to the n-th unit, a plurality of substrates being simultaneously processed by different type of the processing units for one cycle, the system comprising:

a loading/unloading section for taking in and out the substrates;

a first transfer section for receiving/transferring the substrates from/to the loading/unloading section and transferring the substrates one by one to each processing unit;

a second transfer section for receiving/transferring the substrates from/to the processing units; and

a controller for controlling the first transfer section, the second transfer section and the processing units, when the substrates are simultaneously processed by the different types of processing units so that each processing unit processes the substrates one by one within one-cycle time that corresponds at least to either a first total transfer time or a second total transfer time that is larger than the other, the first total transfer time being the total of periods in the one cycle for the first transfer section required for receiving/transferring each substrate from/to the loading/unloading section and transferring the substrate to each processing unit, the second total transfer time being the total of periods in the one cycle for the second transfer section required for receiving/transferring the substrate from/to the processing units.

17. The substrate processing system according to claim 16, wherein

the controller calculates the maximum period among periods  $t_1/m$  to  $t_n/m$  obtained by dividing the periods  $t_1$  to  $t_n$  by the number "m" of the identical units of the first to n-th processing units and sets the maximum among the maximum period, the first total transfer time and the second transfer

time as the one-cycle time for controlling the first and the second transfer sections.

18. The substrate processing system according to claim 16, wherein

at least one of the processing units is a substrate-receiving unit for receiving and processing each substrate, the controller calculating the total receiving and processing period for the substrate-receiving unit for receiving and processing each substrate and setting the maximum among the total receiving and processing period, the first total transfer time and the second transfer time as the one-cycle time.

19. The substrate processing system according to claim 16 further comprising:

an exposing apparatus; and

a third transfer section for receiving the substrates from the processing units and transferring the substrates to the exposing apparatus,

wherein the controller sets the maximum among the first total transfer time, the second total transfer time and a third total transfer time for the third transfer section required for the one cycle, as the one-cycle time.

20. A method of processing substrates with first to n-th processing units ( $n = 1, 2, \dots, N$ ) each having at least one identical unit for performing first to n-th wafer-processing for given periods  $t_1$  to  $t_n$ , respectively, the processing being performed in order from the first unit to the n-th unit, a plurality of substrates being simultaneously processed by different types of the processing units for one cycle, the method comprises the steps of:

processing the substrates one by one in accordance with one-cycle time as a standard time, the one-cycle time being the maximum period among periods  $t_1/m$  to  $t_n/m$  obtained by dividing the periods  $t_1$  to  $t_n$  by the number "m" of the

identical units of the first to n-th processing units; and  
performing processing to each substrate in at least one  
of the processing units with a waiting time.

1. The method of claim 1, wherein the processing units are arranged in a linear array.